REMARKS

Claims 21-40 are all the claims presently pending in this application. Claims 35 and 40 stand rejected on prior art grounds. The Applicant gratefully acknowledges that claims 36-39 would be allowable if rewritten in independent form and that claims 21-34 have been allowed. Claims 36 and 37 (from which claims 38 and 39 depend thereon, respectively) have been rewritten in independent form to place them in immediate condition for allowance. The Applicant respectfully traverses the rejections of claims 35 and 40 based on the following discussion.

I. The Prior Art Rejections

Claim 35 stands rejected under 35 U.S.C. §102(b) as being anticipated by Chevallier, et al. (U.S. Patent No. 6,229,352), hereinafter referred to as Chevallier. Claim 40 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Chevallier. Applicants respectfully traverse these rejections based on the following discussion.

Chevallier teaches a level detection circuit for monitoring the level of a power supply voltage and producing an output signal at power on for resetting various system elements powered by the supply voltage when the supply voltage reaches a predetermined level. The detection circuit, which is powered by the supply voltage includes a voltage reference circuit which produces a reference voltage having a magnitude which is relatively independent of the power supply voltage. A translator circuit functions to produce a translated voltage indicative of the supply voltage magnitude and which is comparable in magnitude to the reference voltage when the supply voltage is at a suitable level such that the system will accept a power on reset

pulse. A comparator circuit functions to compare the reference voltage with the translated voltage and cause an associated output circuit to issue the reset pulse. The reset circuit typically includes a one shot circuit, the output of which is logically ORed with the amplified comparator output. The amplified comparator output functions to hold the system elements in a reset state at very low supply voltages and the one shot output functions to reset the system elements once the supply voltage is at a sufficiently high level.

The claimed invention, as provided in independent claim 35 includes features, which are patentably distinguishable from the prior art references of record. Specifically, claim 35 recites, "A comparator set to have a pair of trip points corresponding to a voltage value of a rising and falling edge of an input signal, wherein said comparator cycles between an analog configuration and a digital configuration by selective selection of said input signal through a plurality of transmission gates, wherein said comparator controls a delay between rising and falling edge transitions at an output signal of said comparator, wherein said comparator controls a pulse width at said output signal of said comparator, wherein one of said trip points is external to said comparator, and wherein a majority of a cycle time of said comparator is spent in said digital configuration.".

With respect to the rejection of claim 35 as being anticipated by Chevallier, and in particular, Figure 2 of Chevallier. Contrary to the assertion in the Office Action, Figure 2 of Chevallier does <u>not</u> show "a comparator having a pair of trip points corresponding to the falling/rising edges of the input signals comprising a comparator (12), passgates (26, 28) coupled to the input signal."

First, there is only <u>a single trip point</u> for the comparator 12 of Figure 2 in Chevallier and

it is the voltage on signal 15 generated by the Voltage Reference 14. Second, the reason there is only one trip point is that comparator 12 of Figure 2 only responds to a rising edge transition of the Input Signal (V_{CC}) on line 11. This Input Signal is also shown in Figure 3A of Chevallier, and it is particularly noteworthy that it only has a rising edge transition, and not a falling edge transition. Conversely, the Applicant's claimed comparator has two distinct and unique trip points (i.e., a pair of trip points), one associated with the rising edge transition of the input signal and another for the falling edge transition of the input signal. Moreover, the Applicant's claimed comparator operates for both rising and falling edge transitions on the input signal, and the trip points for each transition are different and unique, which as indicated above is contrary to Chevallier.

Also, the Applicant strongly traverses the conclusion reached in the Office Action that, "It is well [known] to one having skills in the art that the comparator cycles between the analog configuration when the input voltage is lower than the threshold voltage and the digital configuration when the input signal is higher than the threshold voltage." First, it appears that the Office Action is rejecting claim 35 based on a theory of obviousness. However, obviousness is not a proper reason for rejection under 35 U.S.C. §102(b). Second, even if claim 35 was rejected under 35 U.S.C. §103(a) for reasons of obviousness, the correct determination is not merely whether one having skills in the art would have considered the invention to be obvious, but rather, the correct test is whether one having ordinary skill in the art would have considered the invention to be obvious.

In this regard, one of ordinary skill in the art would not have consider these features obvious because in an "analog configuration", transistors are biased and operated in the

"saturation" region defined by the following two MOSFET transistor device equations: Vds >= Vgs – Vt, and Vgs > Vt, where Vds is the transistor drain-to-source voltage, Vgs is the transistor gate-to-source voltage, and Vt is the threshold voltage of the transistor. In both equations is the requirement that the input voltage, Vgs, be higher, <u>not lower</u>, than the threshold voltage, Vt, for the device to operate in saturation in the "analog configuration". This is in direct contradiction to the statement above from the Office Action. Furthermore, if the input voltage, Vgs, is lower than the threshold voltage, Vt, this is an indication the device is operating in the "cutoff" region, which means the device is turned <u>off</u>. Cutoff is one of the two operating regions of a transistor in the "digital configuration" and is defined by the equation Vgs ≤ Vt, meaning the input voltage, Vgs, is lower or equal to, <u>not higher</u>, than the threshold voltage, Vt, of a transistor in the "digital configuration". This is also in direct contradiction to the statement above from the Office Action.

It would be more correct to associate the "analog configuration" with the region of operation of the MOSFET transistors used in the circuit, as well as characteristics of the circuit topology. In an analog circuit, MOSFET transistors typically operate in the region know as "saturation", and a characteristic trait of analog circuits is that they contain DC current paths, which means there is a path for current to flow between the power supply and the common ground node. However, digital circuits comprised of MOSFET transistors do not employ static DC current paths. Also, the MOSFET transistors in digital circuits operate in the two regions known as "cutoff" and "linear (or triode)".

Comparator 12 in Figure 2 of Chevallier <u>does not and as a technical matter, cannot</u> cycle between an "analog configuration" and a "digital configuration". It is always in the analog

configuration since there is always a static DC current path through the comparator between the Vcc power supply rail and the common ground node. This continuous DC current path would either be through transistors (36, 34, and 40), or (36, 32, and 38).

Also, the Applicant respectfully traverses the Office Action statement, "Because of the hysteresis provide[d] by the passgates (col. 3, lines 52-55), the feedback signal, the value of the reference voltage, the delay between the rising edge and the falling edge transition at the output signal and the output pulse width is controlled."

First, with respect to the above, those of ordinary skill in the art would confer that the statement from the Office Action is incorrect; that is, it is false to say that the value of the reference voltage is controlled because of the hysteresis provided by the passgates (col. 3, lines 52-55). In fact, the output of the voltage reference circuit 14 on line 15 has nothing to do with hysteresis since after time T1 in Figure 3A of Chevallier, it assumes a static DC voltage level that remains constant and does not change in value.

Second, comparator 12 in Figure 2 of Chevallier does not employ hysteresis in the true meaning of the word. Hysteresis is the quality of a comparator whereby its internal input threshold changes as a function of the applied input (or output) voltage level. In particular, when the applied rising input voltage passes the internal input threshold, the output changes, and the internal input threshold is subsequently reduced so that the applied falling input voltage must return beyond the previous internal threshold before the comparator's output changes state again. This description of hysteresis describes two distinct and unique internal comparator trip points, and the comparator in the Applicant's claimed invention absolutely does have two trip points (contrary to Chevallier) since it is reacts to both rising and falling transitions of the input signal

and definitely employs true hysteresis. Indeed, the comparator 12 in Figure 2 of Chevallier does not and cannot have two trip points and therefore cannot have true hysteresis since its output is only expected to change state due to the rising edge transition of the input signal ("Input Signal" in Figure 3A.) and not the falling edge transition. Chevallier does not utilize true hysteresis because by definition, the internal input threshold or internal input trip point has to change, but in comparator 12 in Figure 2 it is the applied input voltage that is increased as described in column 6, lines 1 to 7 of Chevallier. This is a subtle but important distinction regarding hysteresis. Also, the implementation of true hysteresis in a comparator circuit is evident by the fact that there is a unique trip point or trigger voltage, V^+, for a rising input signal voltage and a unique trip point, V^-, for a falling input signal voltage. The "hysteresis voltage", V_H, is defined as $V_H = (V^+ - V^-)$ as provided by the Applicant's specification. This requirement is nonexistent in the comparator 12 of Chevallier.

Therefore, the Applicant respectfully submits that independent claim 35 is patentable over Chevallier. Furthermore, dependent claim 40 is similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. The Applicant notes that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to claims 35 and 40 and to pass these claims to issuance.

II. Formal Matters and Conclusion

With respect to the objections to the claims, the claims have been amended, above, to

overcome these objections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections and rejections to the claims.

In view of the foregoing, Applicants submit that claims 21-40, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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